Lab 4

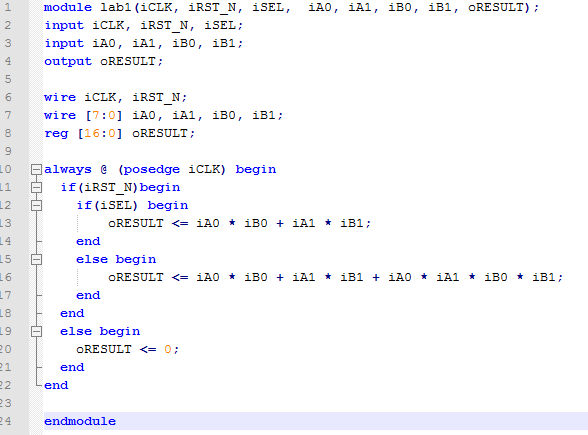
The goals of this lab:

* Synthesize a netlist fom Verilog Code
* Analyze the timing, power and area of the resulting circuit.

Synthesis of the Verilog Code:

First, we had to make modifications to our original code from lab so we will have D flip flops storing the input variables.

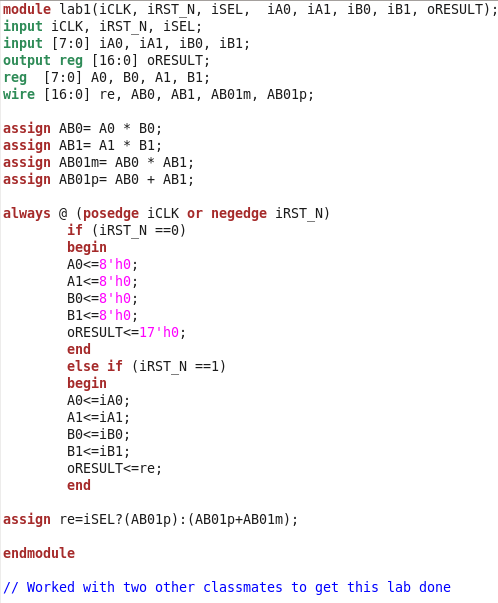
Here is the Verilog file from lab 1:



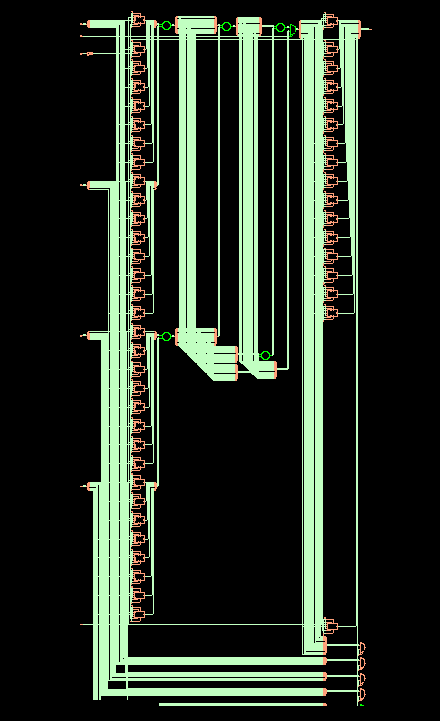
We In order to make this work, we had to modify a few things. We did this with the help of some classmates.

First, we changed the inputs A0 and 1 and B0 and 1 into registers. By doing this, we create d flip flops at the input. But since we did this, we now need intermediate wire variables to carry out the computation. So we add AB0, AB1, ABO1m(product) and AB01p(sum). Then finally the result register is input by the multiplexed wires from the product or sum value.

The resulting code is as follows:



Now that we have code that will synthesize properly, we synthesized the Verilog code and it looks like the image on the next page.

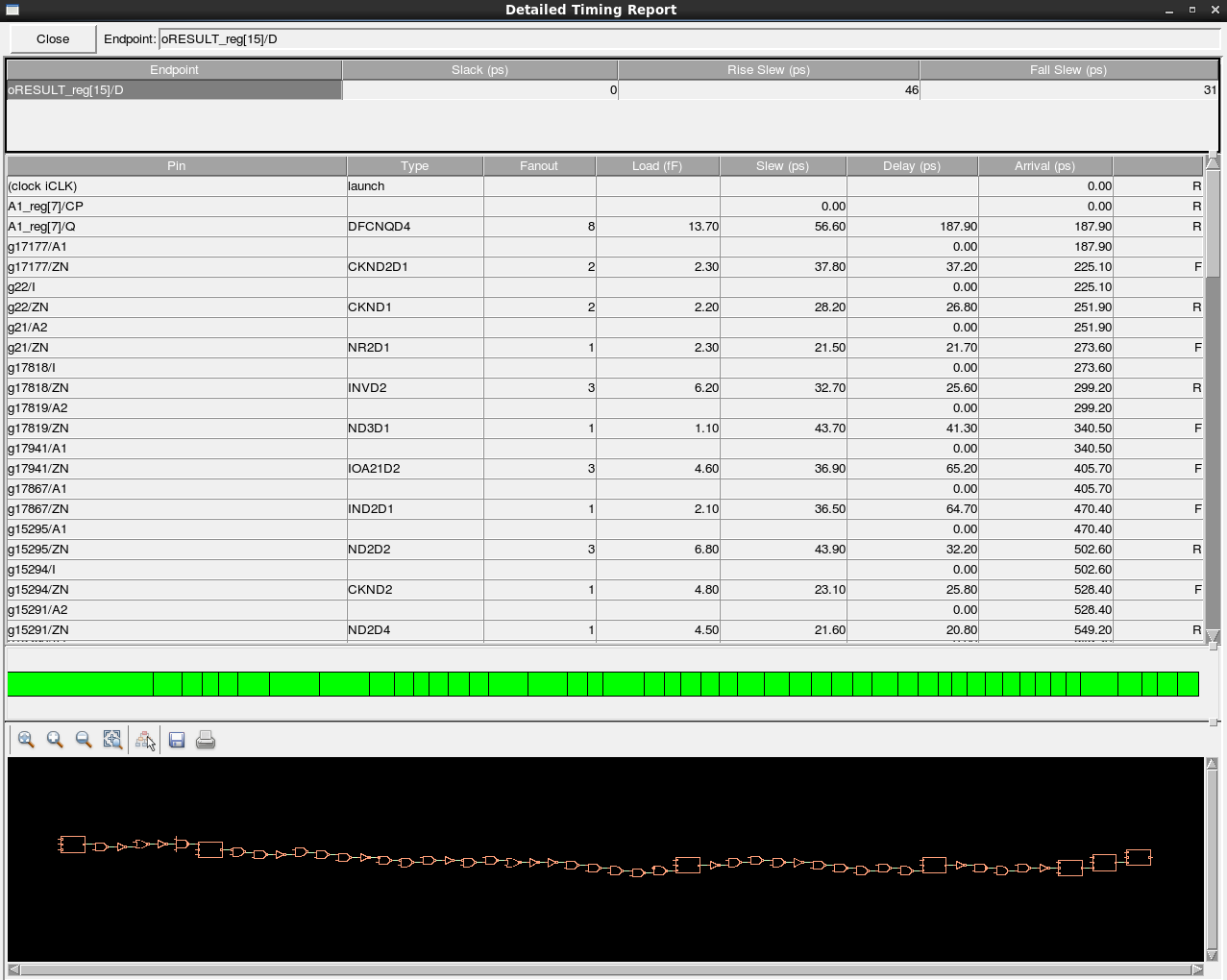


Timing Analysis:

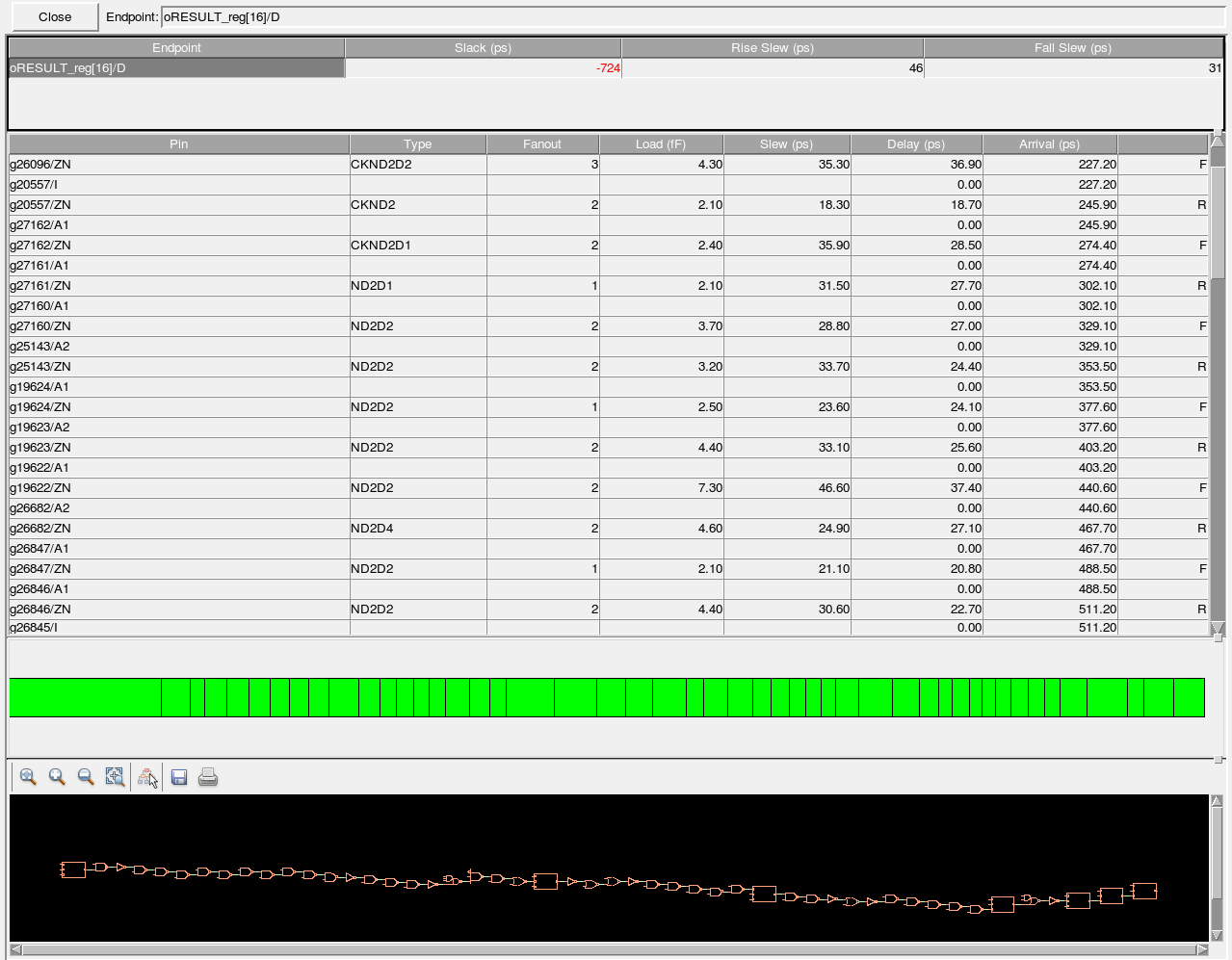
When we ran the timing report we received the following results:

Timing

Report:

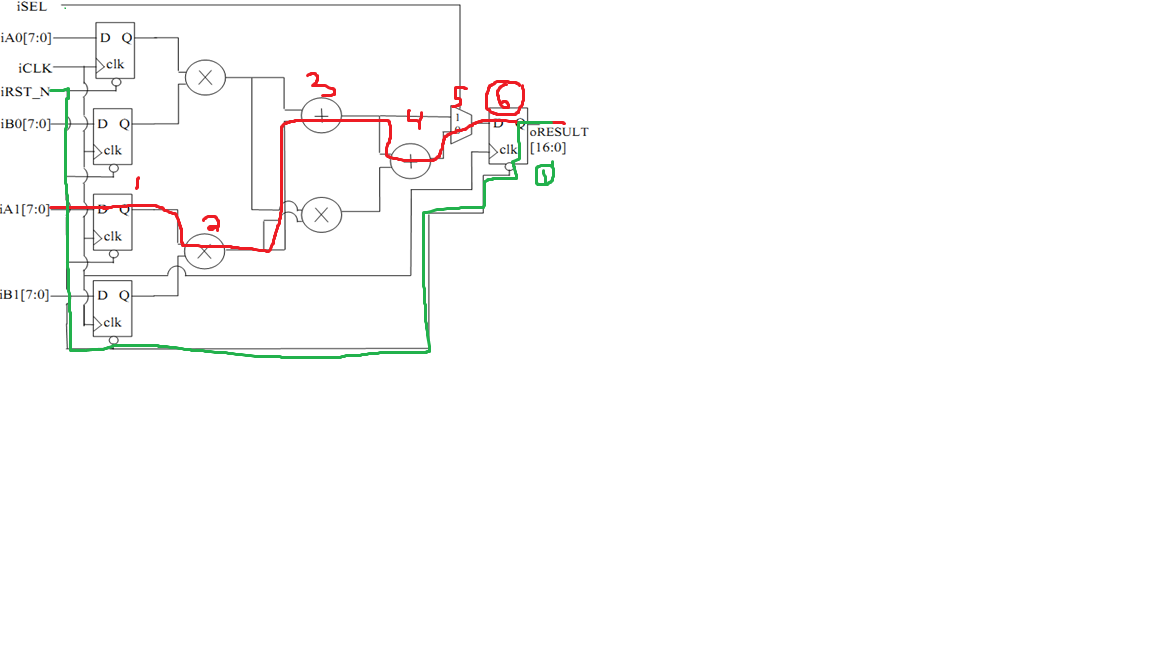


From this, we get a slack value of 0. This means the signal reaches the output at exactly the correct time no later or no earlier. That means this will not be a timing violation. This clock frequency should be the heist possible frequency without error.

Detailed report with FA1D:

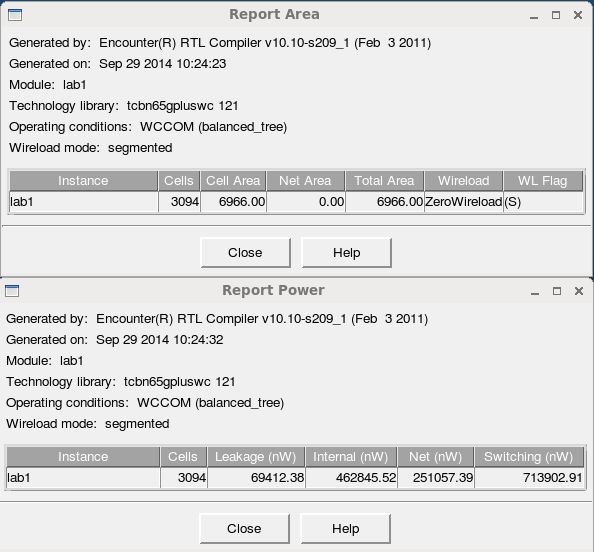
The slack time for this timing analysis is -724ps. This means this will not pass the design check for timing. The clock period is

Slack does not improve when FA1D is used.

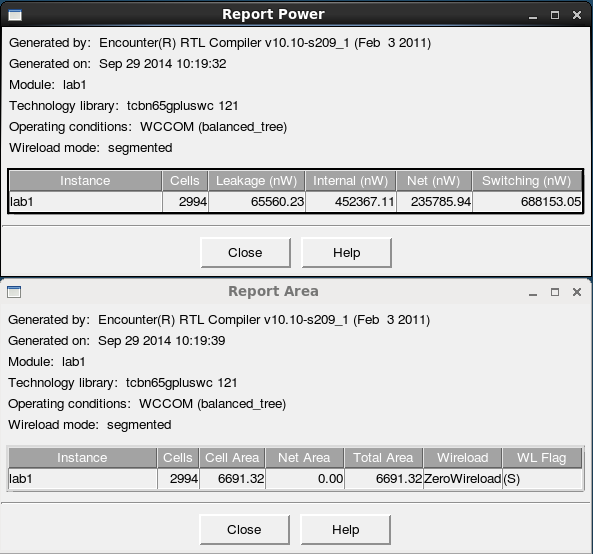


Area and Power consumption analysis:

The area analysis of the first synthesis: (without FA1D and at 1.6ns period)



Comparing these to the area and power report with FA1D below,



We can see that with FA1D there is a slightly smaller area and power consumption.

Conclusion:

In this lab we synthesized our circuit using a few different methods. One being pure synthesis and the other using FA1D standard cells. We discovered that the FA1D method will result in a slower circuit but will have a smaller area and consume less power. So there are trade-offs for both options.